REMARKS

Claims 1-6 and 8-21 are pending. Claims 12-21 are allowed.

The Examiner rejected claim 1 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,710,772 to Sato in combination with U.S. Patent No. 6,286,122 to Alanara. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP § 2143. The combination of Sato and Alanara fails to teach or suggest every limitation of claim 1.

Claim 1 recites:

> A method of classifying a received data frame as being a Discontinuous Transmission (DTX) high or low class, each of said classes having a corresponding format wherein a known bit pattern is located in a different respective position within said data frame, said method comprising:
>
> receiving said frame;
>
> computing a first value representing a confidence-weighted correlation between said known bit pattern and data from a first position of said frame; and
>
> classifying said frame as being a DTX-high or DTX-low class based on said first value.

The Examiner asserted that Sato teaches

> computing a first value (column 6 lines 23-25 and lines 53-57, where the computed value is the data length of the time slot) representing a confidence-weighted correlation between said known bit ***length*** and received data of said frame ((Fig. 1(b) for uplink - active speech period, known bit length is 324 bits, Fig.1 (c) for uplink -silent period, known bit length is 68 bits), wherein the calculated value 68 bits or 324 bits representing a confidence-weighted correlation, a silent period or active speech period.)

Office Action, p. 3, second paragraph (bold emphasis added).

Claim 1 recites a known bit ***pattern***, not a known bit ***length***. A known bit pattern is a predetermined (known) sequence of 1's and 0's, in a predetermined (known) order. A bit length is a cardinal number (such as 68 or 324) resulting from a count of the number of bits in a frame.

Knowing a bit length says nothing about the pattern of those bits. A 68-bit frame may assume any of $2^{68} = 2.95 \times 10^{20}$ bit patterns, and a 324-bit frame may assume any of $2^{324} = 3.42 \times 10^{97}$ bit patterns. The Examiner is entitled to give claim terms their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (emphasis added). MPEP § 2111. No one of skill in the digital arts would conflate a known bit length with a known bit pattern. At most, a known bit length places only an outer bound on the number of different bit patterns that may be represented. Equating the claimed known bit pattern to a known bit length is improper claim interpretation. For at least this reason, the § 103 rejection of claim 1 is improper and must be withdrawn.

Furthermore, claim 1 recites that the known bit pattern is located in a different respective position within each class of data frame. This recitation is also clear to those of skill in the digital arts. According to the plain language of the preamble of claim 1, DTX-high and DTX-low classes of data frames each include the same known bit pattern – a predetermined sequence of 1's and 0's. This known bit pattern is located in a different position within a DTX-high data frame than it is within a DTX-low data frame. It is nonsensical to say that a bit length of a data frame is located in any position of the data frame. This is further evidence that conflating a known bit length to a known bit pattern is improper claim interpretation.

Alanara discloses a method of alerting a base station that a mobile station is about to enter discontinuous transmission (DTX) mode, by transmitting a DTX Trailer word in an unused portion of the penultimate frame prior to DTX. In one embodiment, Alanara's mobile station transmits a known bit pattern and specifies a maximum number of bit errors. The known bit pattern is transmitted with ½ rate or ¼ rate convolutional coding, or no channel coding. At the base station, the received data are compared to the known bit pattern, and a DTX mode indicator is assumed if the received data matches the known bit pattern to within the

predetermined number of bit errors (to allow for noisy channel conditions). This is simply transmitting a predetermined flag as an indicator, and allowing some error margin in receiving and decoding the flag.

Applicants' specification, at p. 6, line 14 – p. 7, line 15, discloses the use of soft bits to enhance correlation confidence. In particular,

> Comparing the reference CDVCC_R 40 [a known bit pattern] to the CDVCC_N 26 sub-field of the received burst 14 [a first position within the frame] will indicate whether the received burst 14 is a normal burst 10 or a truncated burst 12. Simply comparing the decoded binary bits of the CDVCC_N 26 to the CDVCC_R 40, *i.e.*, calculating the Hamming distance, will yield the correlation between the bit patterns, offering some indication of the DTX status of the received burst 14. However, according to the present invention, the confidence level of the CDVCC_N 26, as indicated by the magnitude of the soft bits, may additionally be compared to the CDVCC_R 40 bits (wherein the highest confidence level is assumed) to increase the probability of success of the DTX classification of the received burst 14.

p. 7, lines 16-24. The magnitude of CDVCC_N – received data from a first position in the frame – are compared to (correlated with) soft bits of CDVCC_R – the known bit pattern – which, since it is known, are set to the highest confidence level. The claimed confidence-weighted correlation is thus a correlation between the bit patterns, weighted by a confidence factor resulting from comparing soft bit magnitudes for the bit patterns.

Alanara discloses only the first phase of this calculation – counting the Hamming distance between a known bit pattern and received data to yield a correlation between the bit patterns. If the error, or mismatch, between the two is within a predefined number of bit errors, a match is assumed (DTX mode indication). Otherwise, random noise is assumed (a "bad partial frame," col. 7, lines 3-4). Alanara does not teach or suggest the confidence-weighted correlation that additionally considers soft bit magnitude, as recited in claim 1. For at least this additional reason, the combination of Sato and Alanara fails to teach all claimed limitations, and the § 103 rejection of claim 1 is improper and must be withdrawn.

Claims 2-6 and 8-11 depends from claim 1, and include all limitations of their respective parent claim(s). Accordingly, the dependent claims additionally exhibit patentable nonobviousness over the art of record.

The present application was filed over six years ago (November 16, 2001). The first Office Action, citing the Sato reference, was issued on February 8, 2005. Over nearly three years, six Office Actions have issued, each citing Sato. In the face of this extensive, diligent, and thorough prosecution, it is now clear that the present invention is patentably novel and nonobvious over any interpretation of Sato's teachings, and all other cited prior art as well.

Accordingly, prompt allowance of all pending claims is hereby respectfully requested.

Respectfully submitted,

COATS & BENNETT, P.L.L.C.

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Edward H. Green, III
Registration No.: 42,604

1400 Crescent Green, Suite 300
Cary, NC 27518
Telephone: (919) 854-1844
Facsimile: (919) 854-2084